Nikolaos Sketopoulos

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Profile

Focused on advanced integrated circuit design, including static timing analysis, 3D IC methodologies, open-source EDA flows, and circuit optimisation for performance, area, and reliability in challenging environments.

Work Experience

• **Adjunct Lecturer**, ***Digital Systems, University of Thessaly***
Sep 2025 –Feb 2026 | Larisa, Greece
Responsibilities: Main lecturer of Hardware Systems Design (E702) and Systems Design and Simulation (E703) courses, Code 8307 - MIS 6034651.

• **Postoctoral Researcher**, ***Electrical and Computer Engineering, University of Thessaly***
Jun 2025 –Present | Volos, Greece

• **Co-Founder**, ***Silicon Highway Technologies***
May 2023 –Present | Volos, Greece
Responsibilities: As Co-Founder, I play a pivotal role in conceptualizing, developing, and scaling the business. I lead strategic planning, business development, and financial management while overseeing product development, marketing, and customer acquisition strategies. I also focus on building and managing a high-performing team, fostering a collaborative startup culture, and ensuring operational efficiency to achieve company goals and drive sustainable growth.

• **Adjunct Lecturer**, ***Electrical and Computer Engineering, Aristotle University of Thessaloniki***
Noe 2022 –Sep 2023 | Thessaloniki, Greece
Responsibilities: Main lecturer of Digital Design (EE 005) and Digital Hardware Systems I (EE 054) courses, Hiring Program Code 74496 - MIS 5180700.

• **Military Service**, ***Greek Army (Department of Research and Computer Science)***
Sep 2021 –Sep 2022 | Thessaly
Responsibilities: Technical support for military systems and staff training on software programs.

• **Interim Engineering Intern**, ***Qualcomm***
Mar 2021 –Aug 2021 | Remote
Responsibilities: Worked as an R&D researcher on in-house timing and power analysis tools. Also prepared training materials and presentations on 3D integration to educate engineers on 3DIC technologies.

• **Laboratory Assistant**, ***Electrical and Computer Engineering, University of Thessaly***
Feb 2018 –Jun 2018 | Volos, Greece
Responsibilities: Served as a laboratory assistant for the System-on-Chip (SoC) course (CE330).

• **Laboratory Assistant**, ***Electrical and Computer Engineering, University of Thessaly***
Sept 2015 –Feb 2021 | Volos, Greece
Responsibilities: Served as a laboratory assistant for the Digital Circuit Lab course. (CE333).

• **EDA Researcher, Developer, and Tester**, ***Qualcomm***
Jan 2015 –Oct 2019 | Remote
Responsibilities: I was an external contractor researcher. My responsibilities were to develop, test, and evaluate a Floorplanning and Placement EDA Tool. The EDA tool's functionality includes GUI, I/O, Floorplanning and Standard-Cell Placement Algorithms.

• **Research Associate**, ***Circuit And Systems (CAS) Lab, University of Thessaly***
Apr 2014 --Present | Volos, Greece

Responsibilities: I am a Research Assistant in Electronic Design Automation R&D. The main R&D projects are listed in topics: Clustering, Placement and Routing, 3DIC Placement, Partitioning, Radiation Hardening Placement, Structural Data-path Placement, and GUI Development. Moreover, I supervise undergraduate students in the same fields by providing technical and research support, scheduling future project strategies, and training new researchers. In the context of my mentoring duties, I coordinate several summer internships (2015, 2018-2020), organized by the laboratory.

• **Intern**, ***Helic Inc.***
Jul 2013 --Aug 2013 | Volos, Greece

Trained in Synopsys Design Compiler and IC Compiler, with a focus on clock tree synthesis (CTS) methodologies using industry-standard tools.

Academic Record

• ***Ph.D. in Electrical and Computer Engineering***
2016 --2021 | University of Thessaly, Greece

Thesis: "3DIC CAD Placement Flows and Algorithms Yielding Improved PPA, Supporting MIV Constraints"

Link: https://freader.ekt.gr/eadd/index.php?doc=50170&lang=el

Subject: Investigation of different strategies for Three-Dimensional Integrated Circuits (3DIC), by utilizing existing industrial P&R tools. Techniques such as 3D legalization, clustering, floorplanning, and partitioning are used to control the inter-tier connectivity and improve Power, Performance, and Area (PPA) results of a 3DIC compared to the conventional 2D integration.

• ***MSc in Electrical and Computer Engineering (1 year degree)***
2015 --2016 | University of Thessaly, Greece

Dissertation: "Electronic Design Automation Algorithms for Standard Cell Legalization in Microelectronic Circuits"

Link: http://hdl.handle.net/11615/45971

Subject: Implementation of a standard cell legalizer able to handle Hard Macros and multi-row height cells. The legalizer is an independent part of an EDA tool, while it is quite fast even for large industrial circuits.

• ***M.Eng in Electrical and Computer Engineering (5 years degree)***
2009 --2015 | University of Thessaly, Greece

Dissertation: "Electronic Automation Algorithms for Standard Cell Placement in Microelectronic Circuits"

Link: http://hdl.handle.net/11615/45881

Subject: Research and analysis of standard cell placement legalization followed by the implementation of a placement legalization algorithm written in the C language.

R&D Projects

• ***TWIN-RELECT: Twinning for Excellence in Reliable Electronics***
May 2024 - Present | Horizon Europe 2021-2027 - University of Thessaly, Greece, (code: *7795*)
• ***Asynchronous Static Timing Analysis***
Jun 2023 - Sep 2023 | Niobium Microsystems - University of Thessaly, Greece, (code: *7339*)
• ***Circuit Training Partitioning***
Jan 2022 - Oct 2022 | Google - University of Thessaly, Greece, (code: *7250*)
• ***Software Tool for SET Generation, Propagation using Industrial STA***
Jul 2021 - Dec 2021 | IHP Microelectronics - University of Thessaly, Greece, (code: *6824*)
• ***Qualcomm Faculty Award 2021-2022***
Jan 2021 - Nov 2021 | Qualcomm - University of Thessaly, Greece, (code: *6809*)
• ***Automated Structured Placement (ASP)***
Apr 2018 - Mar 2019 | Qualcomm - University of Thessaly, Greece, (code: *5633*)

Peer Reviewed Journal Publications

• Wang, L., Xing, W. W., Wang, Z., Sotiriou, C., Sketopoulos, N., Xu, N., & Cheng, Y. (2025). ASAP: Accelerating Corner-Based Timing Analysis with Bayesian Active Self-Attention Neural Process. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.
https://doi.org/10.1109/TCAD.2025.3581474
• Garyfallou, D., Simoglou, S., Sketopoulos, N., Antoniadis, C., Sotiriou, C., Evmorfopoulos, N., & Stamoulis, G., (2021). Gate Delay Estimation with Library Compatible Current Source Models and Effective Capacitance. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 29 (5), 962-972.
https://doi.org/10.1109/TVLSI.2021.3061484
• Simoglou, S., Xiromeritis, N., Sotiriou, C., & Sketopoulos, N. (2020). Graph-based STA for asynchronous controllers. Integration, 75, 91-101.
https://doi.org/10.1016/j.vlsi.2020.05.005

Peer Reviewed Conference Publications

• Vamvakidis, D., Georgakidis, C., Tsilingiri, A., **Sketopoulos**, N., Sotiriou, C. P., & Pavlidis, V. F. (2025, July). 3DPlace: Timing-driven Detailed Placement for Monolithic 3D ICs. In 2025 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (Vol. 1, pp. 1-6). IEEE.
https://doi.org/10.1109/ISVLSI65124.2025.11130341
• Tsalapatas, D., Chatzivangelis, N., Sotiriou, C. P., & **Sketopoulos**, N. (2025, May). Post-Placement Timing Optimisations on Asynchronous Designs. In 2025 29th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC) (pp. 126-134). IEEE.
https://doi.org/10.1109/ASYNC65240.2025.00025
• Pavlidis, C., **Sketopoulos**, N., Sotiriou, C. P., & Pavlidis, V. F. (2024, July). Ternary Clock Tree Synthesis for 3D ICs. In 2024 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) (pp. 1-4). IEEE.
https://doi.org/10.1109/SMACD61181.2024.10745448
• Sotiriou, C. P., Goudroumanis, G. R., **Sketopoulos**, N., & Georgakidis, C. (2024, April). Swarm-A VLSI Timing, Fanout-aware Clustering Algorithm. In 2024 25th International Symposium on Quality Electronic Design (ISQED) (pp. 1-8). IEEE.
https://doi.org/10.1109/ISQED60706.2024.10528366
• Georgakidis, C., Sotiriou, C., **Sketopoulos**, N., Krstic, M., Schrape, O., & Breitenreiter, A. (2020, July). R-Abax: A Radiation Hardening Legalisation Algorithm Satisfying TMR Spacing Constraints. In 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (pp. 316-321). IEEE.
https://doi.org/10.1109/ISVLSI49217.2020.00065
• Simoglou, S., Sotiriou, C., Valiantzas, D., & **Sketopoulos**, N. (2020, July). STA for Mixed Cyclic, Acyclic Circuits. In 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (pp. 392-397). IEEE.
https://doi.org/10.1109/ISVLSI49217.2020.00078
• **Sketopoulos**, N., Sotiriou, C., & Pavlidis, V. (2020, July). Metal Stack and Partitioning Exploration for Monolithic 3D ICs. In 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (pp. 398-403). IEEE.
https://doi.org/10.1109/ISVLSI49217.2020.00079
• Georgakidis, C., Paliaroutis, G. I., **Sketopoulos**, N., Tsoumanis, P., Sotiriou, C., Evmorfopoulos, N., & Stamoulis, G. (2020, March). A layout-based soft error rate estimation and mitigation in the presence of multiple transient faults in combinational logic. In 2020 21st International Symposium on Quality Electronic Design (ISQED) (pp. 231-236). IEEE.
https://doi.org/10.1109/ISQED48828.2020.9137014
• Sotiriou, C. P., **Sketopoulos**, N., Nayak, A., & Penzes, P. (2019, November). Extraction of Structural Regularity for Random Logic Netlists. In 2019 Panhellenic Conference on Electronics & Telecommunications (PACET) (pp. 1-7). IEEE.
https://doi.org/10.1109/PACET48583.2019.8956275
• Sakellariou, A., Valiantzas, D., Sotiriou, C., Xiromeritis, N., & **Sketopoulos**, N. (2019, November). Linear Time S-Component Extraction for General Petri Nets. In 2019 Panhellenic Conference on Electronics & Telecommunications (PACET) (pp. 1-6). IEEE.

https://doi.org/10.1109/PACET48583.2019.8956294
• Xiromeritis, N., Simoglou, S., Sotiriou, C., & **Sketopoulos**, N. (2019, July). Graph-Based STA for Asynchronous Controllers. In 2019 29th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS) (pp. 9-16). IEEE.
https://doi.org/10.1109/PATMOS.2019.8862081
• **Sketopoulos**, N., Sotiriou, C. P., & Samaras, V. (2019, May). Investigation and Trade-offs in 3DIC Partitioning Methodologies: In Proceedings of the 2019 on Great Lakes Symposium on VLSI (pp. 451-455).
https://doi.org/10.1145/3299874.3319487
• **Sketopoulos**, N., Sotiriou, C., & Simoglou, S. (2018, March). Abax: 2D/3D legaliser supporting Look-ahead Legalisation and Blockage strategies. In 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE) (pp. 1469-1472). IEEE.
https://doi.org/10.23919/DATE.2018.8342243

Technical Reports

• Moustakidis, S., Liakos, K., Georgakilas, G., **Sketopoulos**, N., Seimoglou, S., Karlsson, P., & Plessas, F. (2020). A novel holistic approach for hardware trojan detection powered by deep learning (HERO). Attract'20.
https://attract-eu.com/wp-content/uploads/2019/05/HERO_ATTRACT.pdf
• Nikolaos **Sketopoulos**, Christos Sotiriou, Stavros Simoglou, Abax: 2D/3D Legaliser Supporting Look-Ahead Legalisation and Blockage Strategies, Technical Report UTH: TR-2017-001, 2018,
https://www.e-ce.uth.gr/wp-content/uploads/formidable/59/Abax-Tech-Report.pdf

Fellowships/Awards

• First Place Award from **TAU Workshop Contest** on "Delay Calculator Using Current Source Model" - 2020
https://www.tauworkshop.com/2020/contest.shtml
• One year scholarship from the organization "ΔEKA", of the **University of Thessaly**, for Ph.D. students' financial support - 2019

• Beneficiary of **Electrical and Computer Engineering Department** Master studies Fellowship (Based on ranking) - 2016

Technical Program Committees/Peer Reviewer

SMACD'24, TCAD'24, TCAD'23

Professional Memberships

IEEE Member, 2018–present
IEEE Young Professionals Member, 2018–present

Hard Skills

Languages:

Greek (Native), **English** (Fluent)

Programming Languages:

C (Advanced), **Verilog** (Experienced), **JAVA** (Experienced), **Python** (Basic)

Operating Systems:

Linux (Advanced), **Microsoft Windows** (Advanced)

Development Tools:

Xilinx ISE (Experienced), **Eclipse** (Experienced), **Sublime** (Experienced), **Make Files** (Basic), **Microsoft Visual Studio** (Experienced)

Other Hard Skills and Tools:

Git, **Valgrind**, **TCL**, **Technical Writing**,
EDA Tools and Flows, **Cadence Innovus**,
Synopsys Design Compiler, **Synopsys IC Compiler**,
Strong Background on Physical Design P&R Algorithms,
Strong software engineering and data structures,
FPGA Programming, **Asynchronous Circuits**

Soft Skills

Effective in conveying complex concepts
Problem-solving and Innovating
Team player and able to work independently
Self-Motivated and Passionate
Analytical and Meticulous

Interests

Interests: Competitive handball (13 years, national level), coaching, certified referee; hiking and cultural travel.